AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Original) A data storage device preamplifier circuit, comprising:

a write amplifier having an input and an output;

a read amplifier having an input and an output; and

a loopback circuit that selectively connects said output of said write amplifier to said output of said read amplifier.

2. (Currently Amended) The data storage device preamplifier circuit of Claim 1 wherein said write amplifier amplifies ~~said~~ a write signal that is received from a read channel circuit and outputs said amplified write signal to a read/write device and wherein said read amplifier amplifies ~~said~~ a read signal that is received from the read/write device and outputs said amplified read signal to the read channel circuit.

3. (Original) The data storage device preamplifier circuit of Claim 2 wherein said loopback circuit includes at least one of a switch and a multiplexer that selectively connects said output of said write amplifier to said output of said read amplifier.

4. (Original) The data storage device preamplifier circuit of Claim 3 further comprising a trigger circuit that controls said at least one of said switch and said multiplexer.

5. (Original) The data storage device preamplifier circuit of Claim 3 wherein at least one of said switch and said multiplexer is controlled by a write enable signal that is generated by the read channel circuit.

6. (Original) The data storage device preamplifier circuit of Claim 1 wherein said read amplifier is shut down when said loopback circuit connects said output of said write amplifier to said output of said read amplifier.

7-10. (Cancelled)

11. (Original) A read channel circuit for a data storage device, comprising:

a first counter that generates a first count of an attribute of a write signal that is output by said read channel circuit; and

a second counter that generates a second count of said attribute of a looped-back write signal that is received by said read channel circuit.

12. (Original) The read channel circuit of Claim 11 further comprising a comparator that compares a difference between said first count and said second count to a threshold and that outputs a first state when said difference is less than said threshold and a second state when said difference is not less than said threshold.

13. (Original) The read channel circuit of Claim 11 wherein said read channel circuit generates a write enable signal that is output to a preamplifier circuit to enable a loopback mode of the preamplifier circuit.

14. (Original) The read channel circuit of Claim 11 wherein said attribute is at least one of a rising edge, a falling edge and a pulse.

15. (Cancelled)

16. (Previously Presented) A read/write path for a data storage device, comprising:

a read channel circuit; and

a preamplifier circuit that communicates with said read channel circuit and that includes a loopback circuit,

wherein said preamplifier circuit includes:

a write amplifier that amplifies a write signal from said read channel circuit and that outputs said amplified write signal to the data storage device; and

a read amplifier that amplifies a read signal received from the data storage device,

wherein said loopback circuit communicates with said write amplifier and said read amplifier and selectively provides a loopback path to test the operation of said write amplifier.

17. (Original) The read/write path of Claim 16 wherein said loopback circuit selectively connects an output of said write amplifier to an output of said read amplifier.

18. (Original) The read/write path of Claim 16 wherein said loopback circuit includes at least one of a switch and a multiplexer that selectively connects an output of said write amplifier to said output of said read amplifier.

19. (Original) The read/write path of Claim 16 wherein said read amplifier is shut down when said loopback circuit connects said output of said write amplifier to said input of said read amplifier.

20. (Original) The read/write path of Claim 18 further comprising a trigger circuit that controls said at least one of said switch and said multiplexer.

21. (Original) The read/write path of Claim 18 wherein said read channel circuit generates a write enable signal that controls said at least one of said switch and said multiplexer.

22. (Cancelled)

23. (Previously Presented) The read/write path of Claim 16 wherein said read channel circuit includes:

a first counter that generates a first count of an attribute of a write signal that is output to said preamplifier circuit;

a second counter that generates a second count of said attribute of a loop-back write signal that is received from said preamplifier circuit; and

a comparator that determines an operating condition of the preamplifier circuit based on said first count and said second count.

24. (Original) The read/write path of Claim 23 wherein said comparator compares a difference between said first count and said second count to a threshold and outputs a first state when said difference is less than said threshold and a second state when said difference is not less than said threshold.

25. (Original) The read/write path of Claim 23 wherein said read channel circuit generates a write enable signal that is output to said preamplifier circuit.

26-29. (Cancelled)

30. (Original) The read/write path of Claim 23 wherein said attribute is at least one of a rising edge, a falling edge and a pulse.

31. (Original) A data storage device preamplifier circuit, comprising:

write amplifying means having an input and an output for amplifying a write signal;

read amplifying means having an input and an output for amplifying a read signal; and

loopback means for selectively connecting said output of said write amplifying means to said output of said read amplifying means.

32. (Original) The data storage device preamplifier circuit of Claim 31 wherein said write amplifying means amplifies said write signal that is received from a read channel circuit and outputs said amplified write signal to a read/write device and wherein said read amplifying means amplifies said read signal that is received from the read/write device and outputs said amplified read signal to the read channel circuit.

33. (Original) The data storage device preamplifier circuit of Claim 32 wherein said loopback means includes switching means for selectively connecting said output of said write amplifying means to said output of said read amplifier.

34. (Original) The data storage device preamplifier circuit of Claim 33 further comprising trigger means for controlling said switching means.

35. (Original) The data storage device preamplifier circuit of Claim 33 wherein said switching means is controlled by a write enable signal from the read channel circuit.

36. (Original) The data storage device preamplifier circuit of Claim 31 wherein said read amplifying means is shut down when said loopback means connects said output of said write amplifying means to said output of said read amplifying means.

37-40. (Cancelled)

41. (Original) A read channel circuit for a data storage device, comprising:

first counting means for generating a first count of an attribute of a write signal that is output by said read channel circuit; and

second edge counting means for generating a second count of said attribute of a looped-back write signal that is received by said read channel circuit.

42. (Original) The read channel circuit of Claim 41 further comprising comparing means for comparing a difference between said first count and said second count to a threshold and for generating a first state when said difference is less than said threshold and a second state when said difference is not less than said threshold.

43. (Original) The read channel circuit of Claim 41 wherein said read channel circuit generates a write enable signal that is output to a preamplifier circuit to enable a loopback mode of the preamplifier circuit.

44. (Original) The read channel circuit of Claim 41 wherein said attribute is at least one of a rising edge, a falling edge and a pulse.

45-46. (Cancelled)

47. (Previously Presented) A read/write path for a data storage device, comprising:

read channel means for generating write signals and for receiving read signals; and

preamp means that communicates with said read channel means for amplifying said write signals and said read signals and including loopback means for providing a loopback path for testing said preamp means,

wherein said preamp means includes:

write amplifying means for amplifying a write signal from said read channel means and for outputting said amplified write signal to a read/write device; and

read amplifying means for amplifying a read signal received from the read/write device, wherein said loopback means communicates with said write amplifying means and said read amplifying means,

wherein said loopback means includes switching means for selectively connecting an output of said write amplifying means to an output of said read amplifying means.

48. (Original) The read/write path of Claim 47 further comprising trigger means for controlling said switching means.

49. (Original) The read/write path of Claim 47 wherein said read channel means generates a write enable signal that controls said switching means.

50. (Previously Presented) A read/write path for a data storage device, comprising:

read channel means for generating write signals and for receiving read signals; and

preamp means that communicates with said read channel means for amplifying said write signals and said read signals and including loopback means for providing a loopback path for testing said preamp means,

wherein said preamp means includes:

write amplifying means for amplifying a write signal from said read channel means and for outputting said amplified write signal to a read/write device; and

read amplifying means for amplifying a read signal received from the read/write device, wherein said loopback means communicates with said write amplifying means and said read amplifying means,

wherein said read amplifying means is shut down when said loopback means connects said output of said write amplifying means to said output of said read amplifying means.

51. (Cancelled)

52. (Previously Presented) The read/write path of Claim 47 wherein said read channel means includes:

first counting means for generating a first count of an attribute of a write signal that is output to said preamp means;

second counting means for generating a second count of said attribute of a looped-back write signal that is received from said preamp means; and

comparing means for determining an operating condition of the preamp means based on said first count and said second count.

53. (Original) The read/write path of Claim 52 wherein said comparing means compares a difference between said first count and said second count to a threshold and outputs a first state when said difference is less than said threshold and a second state when said difference is not less than said threshold.

54. (Original) The read/write path of Claim 52 wherein said read channel means generates a write enable signal that is output to said preamp means.

55-58. (Cancelled)

59. (Original) The read/write path of Claim 52 wherein said attribute is at least one of a rising edge, a falling edge and a pulse.

60. (Original) A method for testing operation of a preamplifier circuit, comprising:

generating a first count of an attribute of a write signal;

transmitting said write signal to a write signal input of said preamplifier circuit; and

looping said write signal back to a read signal output of said preamplifier circuit.

61. (Original) The method of Claim 60 further comprising generating a second count of said attribute of said looped-back write signal.

62. (Original) The method of Claim 61 further comprising:

comparing said first count to said second count; and

diagnosing operability of said preamplifier circuit based on said comparison.

63. (Original) The method of Claim 62 further comprising:

generating a difference between said first count and said second count; and

comparing said difference to a threshold.

64. (Original) The method of Claim 63 further comprising signaling non-operability of said preamplifier circuit when said difference is greater than said threshold.

65. (Original) The method of Claim 60 wherein said preamplifier circuit includes a read amplifier and further comprising shutting said read amplifier down during said looping step.

66-69. (Cancelled)

70. (Original) A method for operating a preamplifier circuit having a write signal input and a read signal output, comprising:

receiving a write signal at said write signal input of said preamplifier; and

selectively looping back said write signal to said read signal output.

71. (Original) The method of Claim 70 further comprising amplifying said write signal before said looping back step.

72. (Original) The method of Claim 71 further comprising further amplifying said write signal after said amplifying and loopback steps.

73. (Cancelled)

74. (Original) The method of Claim 70 further comprising shutting down a read amplifier of said preamplifier circuit when said loopback step is performed.

75. (Original) The method of Claim 70 further comprising:

generating a first count an attribute of said write signal that is input to said write signal input of said preamplifier circuit;

generating a second count of said attribute of said write signal output at said read signal output of said preamplifier circuit; and

comparing said first count and said second count.

76. (Original) The method of Claim 75 further comprising:

generating a difference between said first count and said second count;

comparing said difference to a threshold; and

signaling non-operability of said preamplifier circuit when said difference is greater than said threshold.

77-81. (Cancelled)

82. (Previously Presented) A method for operating a preamplifier circuit, comprising:

selectively operating said preamplifier circuit in a write mode;

selectively operating said preamplifier circuit in a read mode; and

selectively operating said preamplifier circuit in a write mode with loopback,

wherein said write mode with loopback further comprises:

receiving a write signal at a write signal input of said preamplifier;

amplifying said write signal; and

looping back said write signal to a read signal output of said preamplifier.

83. (Original) The method of Claim 82 further comprising further amplifying said write signal after said amplifying and loopback steps.

84. (Cancelled)

85. (Original) The method of Claim 82 further comprising shutting down a read amplifier of said preamplifier circuit when said loopback step is performed.

86. (Original) The method of Claim 82 further comprising:

generating a first count an attribute of said write signal that is input to said write signal input of said preamplifier circuit;

generating a second count of said attribute of said write signal output at said read signal output of said preamplifier circuit; and

comparing said first count and said second count.

87. (Original) The method of Claim 86 further comprising:

generating a difference between said first count and said second count;

comparing said difference to a threshold; and

signaling non-operability of said preamplifier circuit when said difference is greater than said threshold.

88-91. (Cancelled)

92. (Previously Presented) A method for testing operation of a preamplifier circuit, comprising:

generating a write signal;

generating a first count of an attribute of said write signal;

receiving a read signal; and

generating a second count of said attribute of said read signal.

93. (Previously Presented) The method of claim 92 wherein said write signal is looped back in said preamplifier circuit as said read signal.

94. (Previously Presented) The method of Claim 92 further comprising:

comparing said first count to said second count; and

diagnosing operability of said preamplifier circuit based on said comparing step.

95. (Previously Presented) The method of Claim 92 further comprising:

generating a difference between said first count and said second count; and

comparing said difference to a threshold.

96. (Previously Presented) The method of Claim 95 further comprising signaling non-operability of said preamplifier circuit when said difference is greater than said threshold.

97. (Previously Presented) The method of Claim 92 wherein said method is implemented by a read channel circuit.

98. (Previously Presented) The method of Claim 92 wherein said method is implemented by a hard disk controller (HDC).

99-104. (Cancelled)